REMARKS

Claim 4 has been amended. No claims have been cancelled. No new claim has been added. Claims 1-8 are pending.

Claim 4 stands objected to due to minor informalities. Claim 4 has been amended to address the issue cited in the outstanding Office Action. Accordingly, the objection to claim 4 should be withdrawn.

Claims 1-3 and 8 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Gowda (U.S. Patent No. 6,115,066). Claims 5-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gowda in view of Kazuo (Japanese Publication 06-260938) and Adieletta (U.S. Patent No. 6,295,546). These rejections are respectfully traversed.

Claim 1 recites: "a plurality of analog-to-digital converters, ... each associated with N logical units of the pixel sensor array, each of said N logical units having including a plurality of pixels, wherein each analog-to-digital converter includes an ADC portion ... and converts said analog signal to a converted digital value indicating the output signal, and said ADC portion stores said converted digital value into one of a plurality of associated storage elements; and N is at least two" (emphasis supplied). Claim 5 similarly recites: "receiving, in a plurality of A/D converter units, a respective plurality of signals from a respective plurality of first logical units, and A/D converting said respective plurality of signals into a respective plurality of converted digital values and storing said respective plurality of converted digital values information in a respective plurality of first storage units" (emphasis supplied) and "receiving, in said plurality of A/D converter units, a respective of signals from a respective plurality of second logical units, adjacent to said first logical units, and A/D converting said respective plurality of signals into a respective plurality of converted digital values and

storing said respective plurality of converted digital values in a respective plurality of second storage units" (emphasis supplied).

Gowda is directed to a image sensor architecture. As shown in Fig. 3, Gowda discloses a image sensor architecture in which the pixels 30 of the image sensor are organized into columns $C_1 \ldots C_n$, wherein each column of pixels is associated with a respective column line $15_1 \ldots 15_n$. Associated with each column line $15_1 \ldots 15_n$ is an A/D converter $40_1 \ldots 40_n$. Each A/D converter $40_1 \ldots 40_n$ is coupled to a register $42_1 \ldots 42_n$. Significantly, each one of the A/D converter $40_1 \ldots 40_n$ is coupled only a respective one of the plurality of register $42_1 \ldots 42_n$. As noted by the Office Action, Gowda further discloses an alternative embodiment in which each A/D converter could be associated with plural column lines. However, even in this alternate embodiment, each A/D converter 40_1 is still only associated with a single associated register 42_1. See column 4, lines 7-12 ("In the alternative, by incorporating a column select switch (not shown) on each column line 15_1-15_n, a smaller number of A/D converters 40 can be utilized, where each A/D converter would be tied to multiple column lines") and Fig. 3 (illustrating a one-to-one correspondence between A/D converters 40_i and registers 42_i). Gowda therefore fails to teach or suggest associating an A/D converter with multiple registers. Accordingly, the image sensor architecture of Gowda does not teach or suggest the above recited portions of the independent claims.

Kazuo is directed to various implementation of an inverter, and discloses a single A/D converter 1 switchably coupled to a plurality of inputs 4a ... 4n, and a corresponding plurality of storage locations 2a ... 2n . As noted by the Office Action, Gowda discloses an image sensor architecture in which each of a plurality of A/D converters is associated with plural column lines. The Office Action then reasons that the claimed invention would be "an obvious designed modification" (Office Action at page 7) from the teachings of Gowda and Kazuo (which discloses a system in which a single A/D converter is associated with multiple registers).

It is respectfully submitted that this conclusion is erroneous and a result of impermissible hindsight. Gowda is directed to a multiple A/D converter system while Kazuo is directed to a single A/D converter system. The systems disclosed by Gowda and Kazuo are not even in an analogous field, as Gowda is directed to a A/D conversion of pixel array signals in an imaging system while Kazuo is directed to the field of inverters. The prior art must suggest the desirability of the claimed invention. MPEP § 2143.01 at 2100-125 (Rev. 1, Feb. 2003) The Office Action has merely alleged that the claimed invention could be achieved by combining "an obvious design variation" of Kazuo's single A/D converter system into the imaging system of Gowda.

Further, a conclusion of obviousness for combining multiple references is improper if the proposed combination changes the principle of operation of any reference. See Id. at page 2100-127. Gowda discloses multiple A/D converters each associated with multiple input signal lines and a single memory location while Kazuo discloses a single A/D converter associated with multiple memory locations. Accordingly, the principles of operation of Kazuo and Gowda are in conflict. Therefore, the conclusion of obviousness reached in the outstanding Office Action is impermissible.

The Office Action additionally cites to Adieletta, however, Adieletta does not cure the above noted deficiency with respect to the teachings of Gowda and Kazuo. Accordingly, independent claims 1 and 5 are believed to be allowable over the prior art of record. Depending claims 2-4 and 6-8 are also believed to be allowable for at least the same reasons as the independent claims.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: March 19, 2004

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Christopher S. Chow
Registration No.: 46,493
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant